CMOS' Advantages over CCD's

What Are CMOS-AP-iSoC (CMOS) Image Sensors?

CMOS stands for Complementary Metal-Oxide Semiconductor, Active Pixel, and Imaging System on a Chip. Plain CMOS processors (or MOS technology invented at Bell Labs) are the architecture of most computer CPUs and memory modules. Image sensors are silicon chips that capture and read light. High-performance CMOS image sensors use "active-pixel" architectures designed at NASA's Jet Propulsion Laboratory (JPL) in Pasadena, California, in the mid 1990s. ISoC is an extension of APS and facilitates the major innovation of performing digital camera functions on-chip.

What Are CCDs?

Charge-coupled devices were the prevailing inherently analog technology in image capture for 30 years. By the late 1990s, however, they are begun to be replaced in key lower resolution applications, such as machine vision, by CMOS image sensors. By 2003 the more advanced CMOS sensors started to appear in still photography digital cameras where they are displacing film and most recently higher performed, lower cost CMOS sensors replaced CCDs in Cell Phones.

Liberty Imaging, LLC (Liberty) initiated a DARPA contract with partner defense contractor Kollmorgen, Inc. in the mid 1990s to design and build a 3-chip camera to utilize an experimental 720p HDTV CMOS-AP-ISoC sensor JPL designed by spinout startup Photobit, Inc. with support from JPL. The six million dollar projects had a very aggressive goal to fast-track CMOS commercialization and develop a 720p studio production camera to introduce HDTV program production. The engineering challenges were formable and not unexpectedly delays were encountered. In the last two years of the Clinton administration the defense budget was severely cut. Faced with hard choices DARPA slashed the budget to $3.2 million which resulted in suspending the project prematurely. JVW

Standard Fabrication Lowers Costs and Enables On-Chip Integration.

CCD sensors rely on specialized fabrication that requires dedicated—and costly—manufacturing processes. In contrast, CMOS image sensors can be made at standard manufacturing facilities that produce roughly 90% of all semiconductor chips today, from powerful microprocessors to RAM and ROM memory chips. This standardization results in vast economies of scale and leads to ongoing process-line improvements. CMOS processes, moreover, enable very large scale integration (VLSI). This advantage is used by "active-pixel" (AP) architectures to incorporate selected camera functions onto the chip. Such integration creates a compact camera system that is more reliable and reduces the number of peripheral support electronics packaging and assembly, further reducing cost.

Low Power Usage Extends Battery Life

Active-pixel architectures consume much less power—up to 100x less power—than their CCD counterparts. CCD systems, on the other hand, tend to be inherently power hungry. This is because CCDs are essentially capacitive devices, needing external control signals and large clock swings (5–15 volts) to achieve acceptable charge transfer efficiencies. Their off-chip support circuitry dissipates significant power. CCD systems require numerous power supplies and voltage regulators for operation.

Random Access to Pixel Regions of Interest Adds Flexibility

In CMOS active-pixel image sensors, both the photo detector and the readout amplifier are part of each pixel. This allows the integrated charge to be converted into a voltage inside the pixel, which can then be read out over X-Y wires (instead of using a charge domain shift register, as in CCDs). This column and row addressability, similar to common DRAM, allows for window-of-interest readout (windowing), which can be utilized for on-chip electronic pan, tilt, and zoom. Windowing provides

much added flexibility in applications that need image compression, motion detection, or target identification and tracking and various recognition security programs.

No Artifacts, Smear, or Blooming Means Higher-Quality Images

With active-pixel architectures, the RMS input-referred noise is comparable to the very high-end (and expensive) CCDs. Both technologies provide excellent imagery compared with other CMOS image sensors. Advanced AP architectures use intra-pixel amplification in conjunction with both temporal and fixed-pattern noise suppression circuitry (i.e., correlated double sampling), which has the potential to produce exceptional imagery in terms of dynamic range (a wide ~75 dB) and noise (a low ~15 e-RMS noise floor), with low fixed-pattern noise (<0.15% sat). AP active-pixel sensors achieve quantum efficiency (sensitivity) that is comparable to high-end CCDs, but, unlike CCDs, they are not prone to column streaking due to blooming pixels. This is because CCDs rely on charge domain shift registers that can leak charge to adjacent pixels when the CCD register overflows, causing bright lights to “bloom” and leading to unwanted streaks in the image. In some AP architectures, the signal charge is converted to a voltage inside the pixel and read out over the column bus, as in a DRAM. Also AP sensors can have built-in anti-blooming protection in each pixel, so that there is no blooming. And smear, caused by charge transfer in a CCD under illumination, can also be avoided.

Intra-Pixel Amplification and On-Chip ADC Produce Faster Frame Rates

CMOS active-pixel designs are inherently fast, which is an advantage in machine-vision and motion-analysis applications particularly. AP can drive an image array’s column buses at greater speeds than is possible on passive-pixel CMOS sensors or CCDs, while on-chip analog-to-digital conversion (ADC) eases the driving of high-speed signals off-chip. A separate benefit of on-chip ADC is the output signal’s low sensitivity to pick-up or crosstalk. This facilitates computer and digital-controller interfacing while adding to system robustness. Additional noise reduction is a further benefit of on-chip ADC as analog degradation is arrested much early in the process.

On-Chip Integrated Circuitry Enables “Smart” Camera Functions

CMOS active-pixel architectures allow signal processing to be integrated on-chip. In addition to the standard camera functions—AGC (Automatic Gain Control), auto-exposure control, etc.—many higher-level DSP functions can be realized. These include anti-jitter (image stabilization) for handheld or unstable camera platform situations, color encoding, computer databus interface circuits, multi-resolution imaging, motion tracking for perimeter surveillance (“smart image sensing”), target recognition, compression, internet distribution and wireless camera control.

Flexibility in a Multimedia Environment

CMOS architectures feature programmability that permits selected functions to be controlled by the camera operator. This capability provides, for the first time, the opportunity to design a broad array of options that are not possible with CCDs. The ability to program the sensor permits any number of innovations that will expand the technology horizontally across industries utilizing broadband internet connectivity to include homeland security, health care, automated manufacturing, e-commerce conferencing, machine vision, automated farming and defense. On chip digital processing leads to a general reduction in size, power consumption, weight, and manufacturing cost and with the advent of wireless wideband networks like LTE management and control systems will be rational to digitally automat industrial infrastructure worldwide from effecting and secure centralized faculties.